Jinzhe Zhang (Zinsser)

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Objective: Jan 2019 Fulltime in **Digital Circuit Design** / **VLSI** / **Architecture** / **ASIC** / **FPGA** / **Physical Design**

Education

- M.S. Electrical Circuits & System. UC San Diego GPA: 3.96 09/2017 ~ 12/2018
- B.S. Electrical and Electronic Engineering (Focus: circuit design, electives: architecture and music)
  UC San Diego Overall GPA: 3.86 09/2013 ~ 06/2017
  MAGNA CUM LAUDE Latin honor and HENRY G. BOOKER MEMORIAL HONORS
- Relevant courses: VLSI Algo&Arch, VLSI Physical Design (P&R), CMOS Analog IC design (Amp, Opamp, SC circuits, ADC)

Skills/Qualifications

- Proficient in digital **Verilog design** (Verilog, Systemverilog), optimizing RTL design
- Proficient in **Python** and **C programming**. Fluent in coding in PHP, C++, html, CSS, JavaScript. Able to use SQL, CUDA, Java, shell script, C#, Matlab, Tcl and any other programming languages with referencing to documentations.
- Fluent in **Embedded system design** and programming.
- Fluent in **Linux system admin**istration, setting up and maintaining servers and clusters.
- Fluent in speaking and writing in **English** and **Chinese**.

Relevant Experience

Chip Test System Design (summer intern), Spreadtrum Communications, Inc. (2018 Summer)
- Designed an FPGA testbench with RF chips as the DUT.
- Implemented custom **LVDS** protocol using Arria V on-chip **transceiver** blocks. (Up to 4Gbps duplex transfer)
- Implemented SPI, JTAG interfaces and memory-mapped registers. Accessing DDR3 with provided IP.
- Simulated testbench with cadence tools and verified the implementation on actual FPGAs.

Superscalar Out-of-order Processor Design (student and TA), UCSD CSE148 (2017/2018 Spring)
- Achieved 2.52 average speed up over scalar pipeline.
- Implemented superscalar out-of-order execution pipeline with register renaming support in Systemverilog.
- TA'ed in the second year, re-designed the entire baseline so that students can implement more types of optimizations.

FPGA SHA-1 Accelerator, UCSD ECE111 (2016 Winter)
- Achieved 1st place for area*latency (6.6% smaller than 2nd place) and 2nd place for latency (2‰ slower than 1st place)
- Implemented SHA-1 hashing algorithm in Verilog. Optimized for latency, through put, area*latency.

Other Experience

Parallel Computation, UCSD CSE260 (2017 Fall)
- Coded and optimized multithreading (Pthread), GPGPU (CUDA), distributed computation (OpenMPI).

Summer intern, ASML - Brion (2016 Summer)
- Wrote python automation script to simulate Photolithography process and run FDTD simulation. This included distributing jobs to LSF-managed clusters. It allows the company to verify products easily with an alternative algorithm.
- Optimized C++ code by migrating to an AVX-compatible build environment. Module performance increased by 200%.

Research assistant, Prime system lab, UCSD (12/2015 to 06/2016)
- Characterized fabricated transistors under different temperatures (up to 600 degrees Celsius).

Teaching assistant, University of California, San Diego (09/2014 to present)
- TA'ed ECE15 (C programming) and CSE148 (Computer architecture). Lead discussion sessions and office hours.

Web development (12/2013 to present)
- Worked with a friend to build a download mirror for a game called Osu! I worked on the backend. Download speed of Chinese players can be boosted up to 1000 times faster. 10k+ users have made 1M+ downloads. (http://status.inso.link/)