Project 1

- Finish Tutorial 1 before starting Project 1.
- Project 1 is the design of a Fibonacci calculator using Verilog HDL.

Fibonacci (cont.)

- F(n) = 0 when n=0
- F(n) = 1 when n=1
- F(n) = F(n-1) + F(n-2) when n>1
- Examples:

F_0	F_1	F_2	F_3	F_4	F_5	F_6	F_7	F_8	F_9
0	1	1	2	3	5	8	13	21	34

Project 1 (cont.)

```
module fibonacci_calculator (
    clk,
    reset_n,
    input_s,
    begin_fibo,
    done,
    fibo_out
);
input [4:0] input_s;
input reset_n ;
Input begin_fibo ;   // Start
    calculation
input clk ;
output done ;
output [15:0] fibo_out;
// Put your code here
//……..
endmodule
```